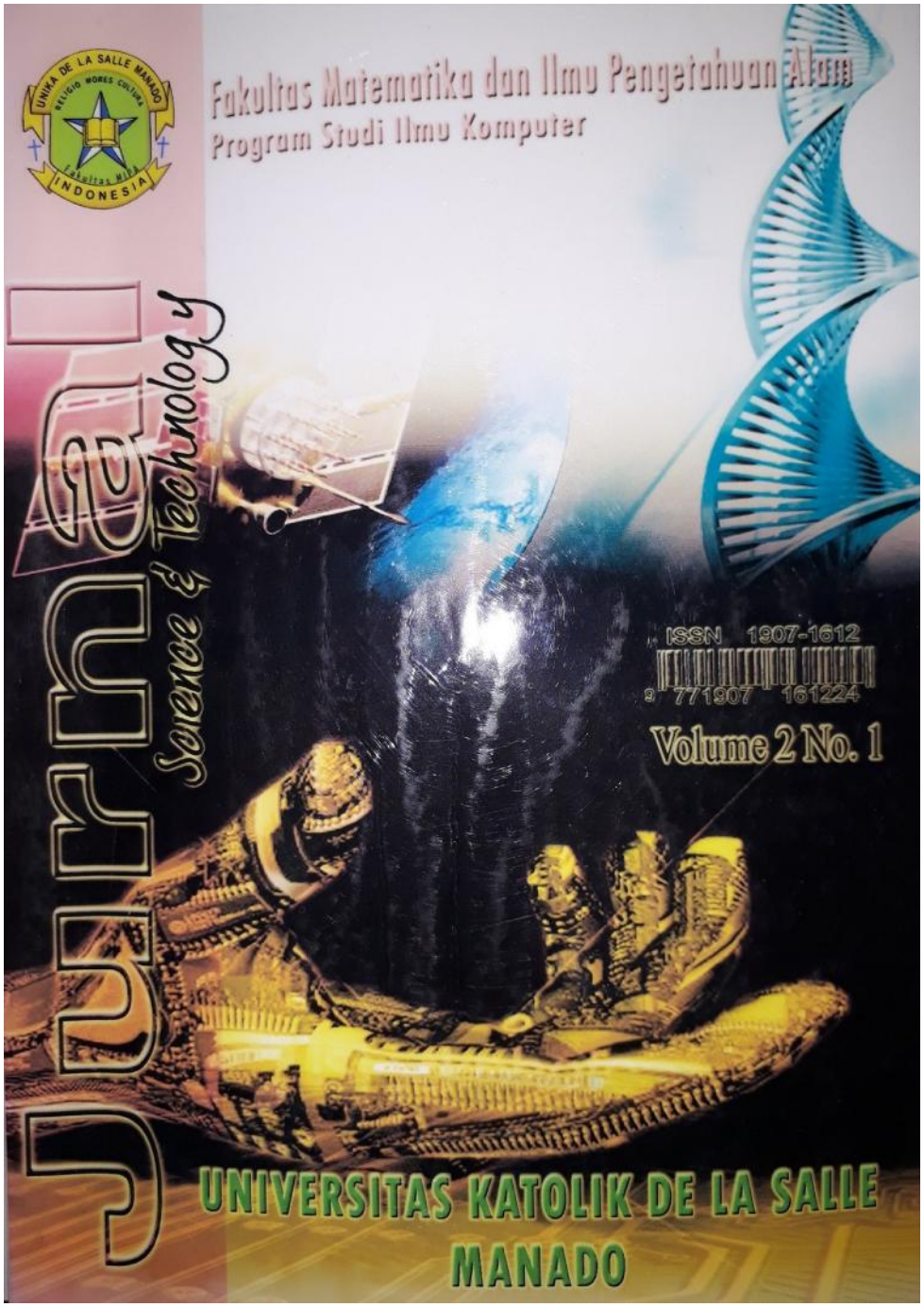

UNIMA DE LA SALLE MANADO
RELIGIO MORES CULTUS
Fakultas MIPA
INDONESIA
Fakultas Matematika dan Ilmu Pengetahuan Alam
Program Studi Ilmu Komputer
Jurnal
Science & Technology
ISSN 1907-1612
9 771907 161224
Volume 2 No. 1
UNIVERSITAS KATOLIK DE LA SALLE
MANADO

SCIENCE & TECHNOLOGY
Jurnal Ilmiah

Jurnal
Science & Technology

ISSN 1907-1612

Volume 2 Number 2
December 2007

Contents

SEQUENTIAL DESIGN OF A BI-FUNCTION SHIFT REGISTER

Lianly Rompis

Abstrak

Register geser merupakan salah satu rangkaian sekuensial yang sangat berperan penting dalam pemrosesan informasi secara digital. Rangkaian sekuensial ini berfungsi untuk menyimpan bit-bit data, yang kemudian dapat ditransfer secara serial maupun paralel. Peranannya yangcukup besar dalam penyimpanan informasi dan pentransferan data mendorong penulis untuk menampilkan implementasi yang lain dari sebuah register geser. Suatu model disain yang mempunyai dua fungsi, yaitu sebagai register geser paralel input paralel output dan juga sebagai register geser paralel input serial output. Diharapkan konsep disain yang baru ini akan bermanfaat dalam proses perancangan teknologi digital, terutama yang berhubungan dengan rangkaian register, serta mampu membangkitkan antusiasme untuk selalu menciptakan teknologi-teknologi yang baik.

Keywords: *Shift Register, Parallel, Serial, Bi-function*

Methods

To build the new design, for shift register, firstly I have to learn and understand the theory of a register, which has the properties of PIPO and PISO. Then I try to derive a combinational circuit for combining these two kinds of function by following the rules of combinational design.

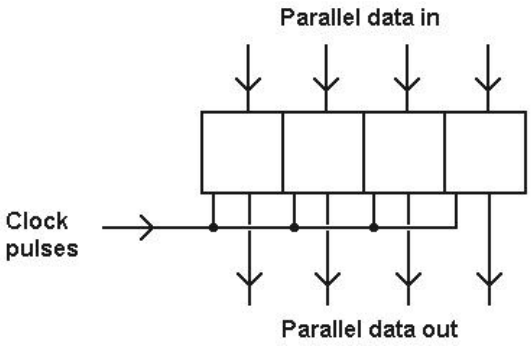
Discussion

A register is a sequential circuit used for storing information in form of data bits. The main component for register circuit is D flip-flop. One flip-flop represents one data bit. If we want to design a register for 32–bit data, we have to use 32 flip-flops. A quite complex circuit that is actually has well–arranged lines to connect to. There are four kinds of register: parallel input parallel output shift register, serial input serial output shift register,

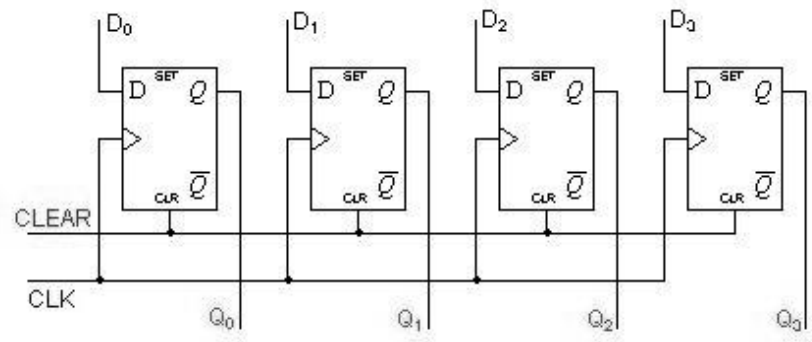
serial input parallel output shift register, and parallel input serial output shift register.

1.1 Parallel Input Parallel Output (PIPO)

This is a type of shift register that stores information in parallel. It has parallel inputs and parallel outputs. Those inputs are also clocked out simultaneously, in parallel.



Picture 1. Diagram of Parallel Input Parallel Output

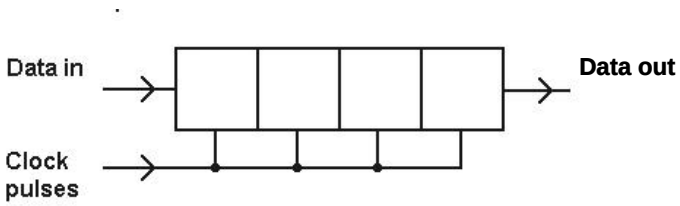


Picture 2. Parallel Shift Register

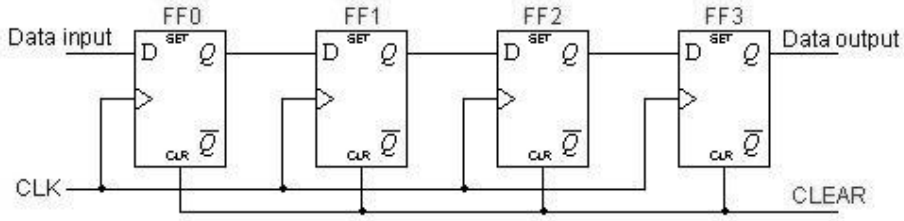
1.2 Serial Input Serial Output (SISO)

This is a type of shift register that stores information in serial. All flip-flop components are arranged in series with simultaneous synchronous clock.

Upon the arrival of a clock pulse, data at the D input of each flip-flop is transferred to its Q output.



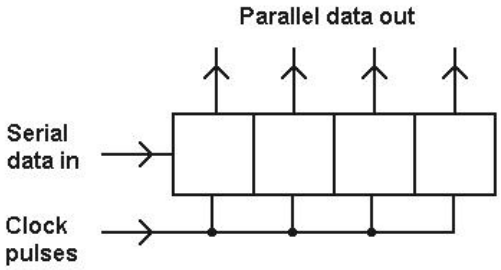
Picture 3. Diagram of Serial Input Serial Output



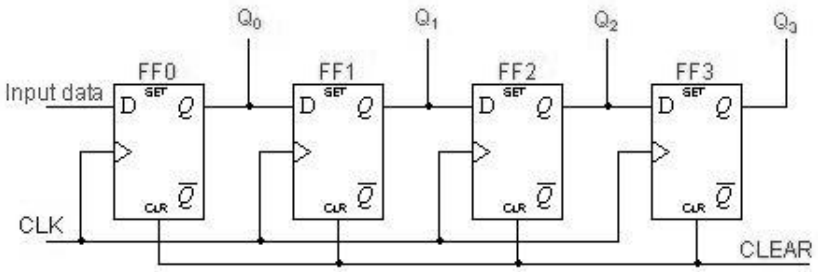
Picture 4. Right Shift Register

1.3 Serial Input Parallel Output (SIPO)

This is a type of shift register that has a serial input and parallel outputs. The data is fed bit by bit into this shift register; in the same way as for the SISO shift register. However the bits are all shifted out simultaneously, in parallel.



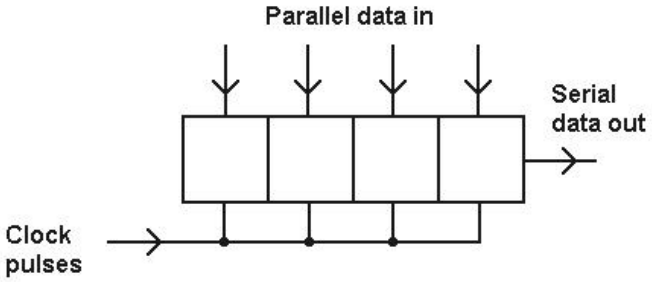
Picture 5. Diagram of Serial Input Parallel Output



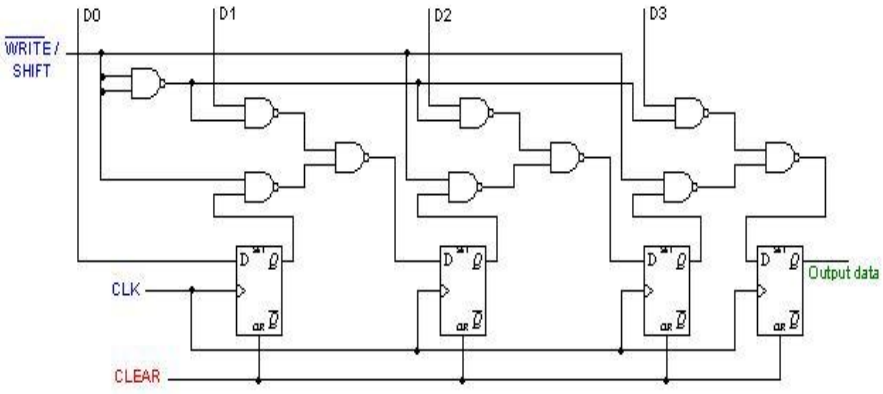
Picture 6. Serial-Parallel Shift Register

1.4 Parallel Input Serial Output (PISO)

This is a type of shift register that has parallel inputs and a serial output. The data is shifted into the register simultaneously, in parallel. They are clocked out, one after the other, in serial form.

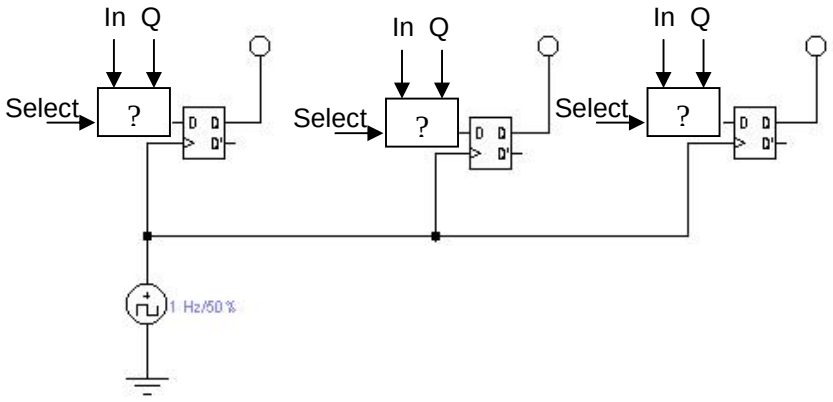


Picture 7. Diagram of Parallel Input Serial Output



Picture 8. Parallel-Serial Shift Register

The type of register that we want to design is a bi-function shift register, which is the combination of a parallel shift register and a parallel-serial shift register. Take the basic form of parallel input serial output shift register that meets this requirement. In this case, there will be a select input to choose one of those two functions. Each data bit represented a D flip-flop and a state Q. This circuit will have n-bit data input and n-bit data output for parallel, and only one data output for serial.



Picture 9. Block Diagram of Combinational Circuit for each FF input

The combinational circuit has three inputs and one output. Make a truth table to derive the logic value for D input.

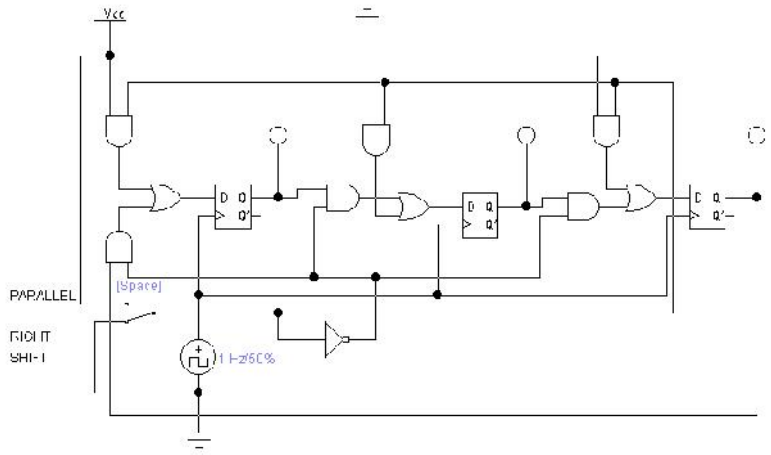
S	In	Q	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Select = logic 1 = parallel shift register
Select = logic 0 = parallel input serial output shift register
In = input = parallel input
Q = current state transition

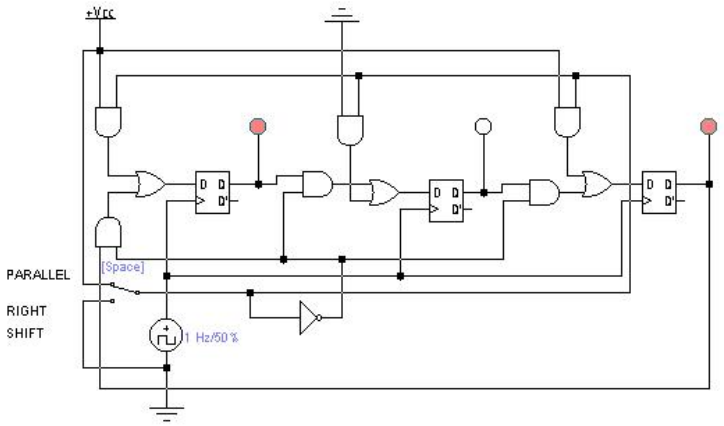
S \ InQ	00	01	11	10
0	0	1	1	0
1	0	0	1	1

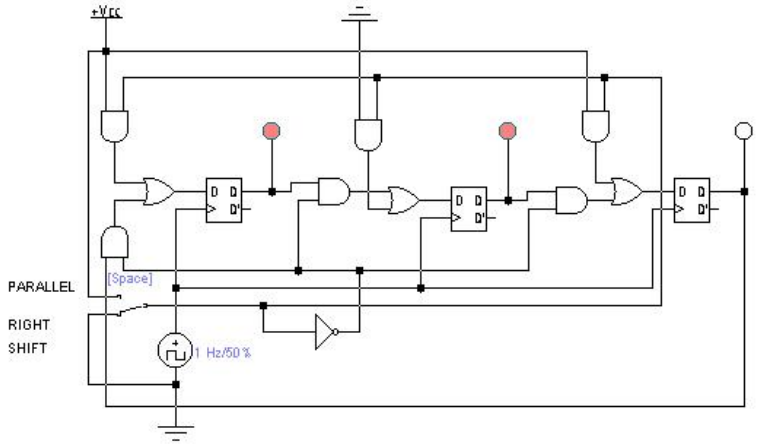
D = S'.Q + S.In

I finally have the solution for each FF inputs. Notice that the state Q is taken from the Q of previous FF. So the complete sequential design for a bi-function register is like the following circuit:



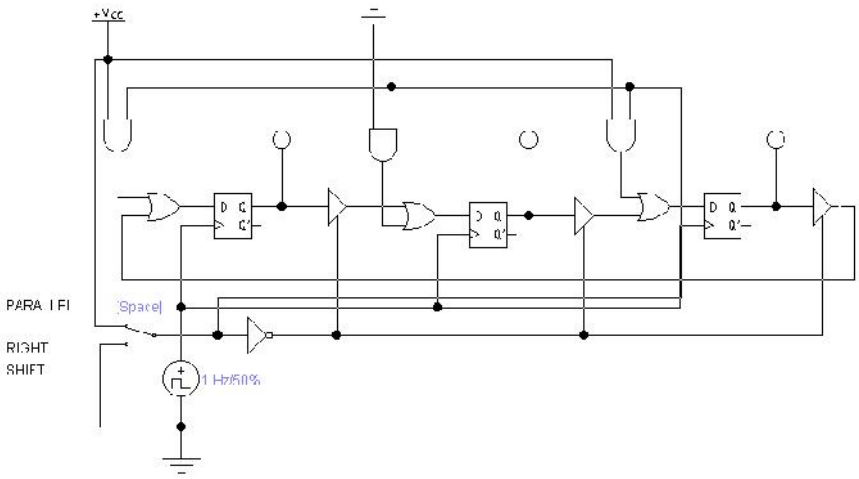
Picture 10. Sequential Design of a Bi-function Shift Register





Picture 11. Simulations using Electronics Workbench 5.12

Another alternative for the same design of a bi-function shift register is like the following one, which is modified using tri-state buffers.



Picture 12. A Bi-function Shift Register modified with Tri-state Buffers

Conclusion

By adding the right combinational circuit for each FF input, we can build a bi-function shift register that could transfers parallel data input into serial or parallel output. Using the same way of design, we are possible to develop another kind of shift register with specific functions.

Acknowledgement

Special thanks to my dearest friend who always support me to keep on going in whatever circumstances, because the life is a most precious gift that we can have.

References

EEE111Digital Systems. http:/www.engj.ulst.ac.uk/

Ibrahim, KF. 1996. *Teknik Digital*. Santosa, P.I. (alih bahasa). ANDI Yogyakarta, pp. 85-90.

Malvino, Albert Paul. 1988. *Elektronika Komputer Digital*. Tjia May On, Ph.D. (alih bahasa). Erlangga Jakarta, pp. 127-132.

Sequential Circuits. http:/ www.eelab.usyd.edu.au/digital_tutorial/

Register Circuits. http://ourworld.compuserve.com/homepages/ g_knott/index1.htm

Tokheim, Roger L. 1996. *Prinsip - Prinsip Digital*. Sutisna (alih bahasa). Erlangga Jakarta, pp. 164-173.